AMENDMENTS

This section presents changes to the specification and the claims in a clean-unmarked format. A version with markings to show the changes made by the current amendment is provided after the remarks section.

In The Claims:

Presented below are the claims in a clean-unmarked format. Please amend claims 1, 6, 16-19, 21-22, 31, 34, 45, and 48-50 as indicated below.

Presentation Of The Claims In A Clean-Unmarked Format

1. (Amended) A system comprising:

an instruction memory to store a plurality of predefined bus stimuli instructions that represent a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases; and

one or more phase generators coupled with a bus and the instruction memory, the one or more phase generators to drive a series of signals on the bus corresponding to the predefined sequence of bus transactions.

3. The system of claim 1, wherein the instructions comprise instruction words having a predefined length.

4. The system of claim 1, wherein the one or more phase generators are further responsive to signals received from the bus.

5. The system of claim 1, further comprising a response memory coupled with the phase generator to store predefined responses to signals received from the bus.

6. (Amended) The system of claim 1, wherein the one or more phase generators includes at least one digital logic device responsive to the instructions and at least one phase engine to control timing of the bus stimuli.

7. The system of claim 6, wherein the digital logic device comprises a field programmable gate array.

8. The system of claim 6, wherein the digital logic device comprises an application specific integrated circuit.

9. The system of claim 6, wherein the at least one digital logic device includes a control portion to provide bus control signals and a data portion to send data to the bus.

10. The system of claim 9, wherein the control portion includes a flow logic device, a request logic device, and a data logic device.

11. The system of claim 6, wherein the at least one phase engine includes at least one logic level translation device.

12. The system of claim 6, wherein the at least one phase engine comprises a system phase engine, an arbitration phase engine, a request phase engine, a snoop/error phase engine, and a data phase engine.

13. The system of claim 9, further comprising a data memory coupled with the data portion.

14. The system of claim 9, wherein the data portion further receives data from the bus.

16. (Amended) A system comprising:

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a first means for storing instructions representing a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases; and

second means for driving the predefined sequence of bus transactions as signals on the bus.

17. (Amended) The system of claim 16, further comprising third means for storing data representing predefined responses to signals received from the bus, and wherein the second means implements the predefined responses based on the signals received from the bus.

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18. (Amended) The system of claim 16, further comprising fourth means for controlling the timing of the signals provided to the bus by the second means.

19. (Amended) The system of claim 16, further comprising fifth means for storing data to be exchanged with agents on the bus, wherein the second means transmits data from the fifth means in response to the instructions stored in the first means.

21. (Amended) A method comprising:

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receiving instruction words representing a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases; and

executing the predefined sequence of bus transactions by converting the instruction words to signals and driving the signals on the bus.

22. (Amended) The method of claim 21, further comprising:

defining a sequence of bus transactions; and

assembling the sequence of bus transactions into instruction words wherein the sequence of bus transactions are executed when the instruction words are converted to signals and driven on the bus.

23. The method of claim 21, further comprising providing predefined signals to the bus in response to signals received from the bus.

24. The method of claim 21, further comprising exchanging data with agents on the bus.

31. (Amended) A method comprising:

generating a plurality of instruction words corresponding to a predefined sequence of bus transactions, wherein each transaction has multiple phases;

storing the instruction words in a memory; and

executing the predefined sequence of bus transactions by converting the plurality of instruction words into signals and driving the signals onto the bus in the predefined sequence.

32. The system of claim 1, further comprising:

an interface other than the bus coupled with the instruction memory, the interface to connect with a device to receive a plurality of predefined bus stimuli instructions.

33. The system of claim 1, wherein the plurality of predefined bus stimuli instructions are to drive a predefined ordered sequence of bus transactions onto the bus.

34. (Amended) A system comprising:

an interface to a host computer to receive a representation of a predefined sequence of bus stimuli associated with multiple phase bus transactions;

a memory to store the representation;

logic to translate the representation into the sequence of bus stimuli; and

a phase generator to provide the predefined sequence of bus stimuli to the bus.

35. The system of claim 34, wherein the sequence is user specified.

36. The system of claim 34, wherein the representation is generated from user specified high level language by an assembler.

37. The system of claim 34, wherein the representation of the bus transaction is generated from a bus functional model by an assembler.

38. The system of claim 34, wherein the representation of the bus transaction is generated from a logic analyzer trace file by an assembler.

39. The system of claim 34, wherein the representation comprises an instruction word having a plurality of segments of predefined length.

40. The system of claim 39, wherein a first segment of the plurality comprises information about a type of the bus transaction, a second segment comprises arbitration information, a third segment comprises transaction data, and a fourth segment comprises memory address information.

41. The system of claim 34, wherein the memory comprises a static random access memory.

42. The system of claim 34, wherein the logic comprises dedicated translation hardware.

43. The system of claim 42, wherein the hardware comprises hardware selected from the group consisting of a field programmable gate array and an application specific integrated circuit.

44. The system of claim 34, wherein the system does not comprise a central processing unit.

45. (Amended) The system of claim 34, wherein the predefined sequence of bus stimuli are correspond to three bus transactions.

46. The system of claim 34, further comprising a connector to connect the system with a processor socket on a motherboard.

47. A bus agent designed by detecting a bug with the system of claim 34 and removing the bug.

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48. (Amended) A system comprising:

a bus to receive bus transactions;

a bus agent coupled with the bus; and

debug means coupled with the bus for asserting a legal sequence of multiple phase bus transactions on the bus and for allowing determination of an incorrect response to the sequence by the bus agent.

49. (Amended) A bus agent designed to eliminate a bug determined by the system of claim 48.

50. (Amended) An integrated circuit designed by defining a legal sequence of multiple phase bus transactions, asserting signals corresponding to the sequence of bus transactions on a bus, capturing a response of an integrated circuit to the sequence of bus transactions, analyzing the response to detect a bug associated with an incorrect response to the legal sequence, and correcting the bug.

51. The circuit of claim 50, wherein the sequence of bus transactions is defined in a high level language.

52. The circuit of claim 50, wherein the integrated circuit is a processor.

53. The circuit of claim 50, wherein the integrated circuit is designed without causing a processor to assert the signals corresponding to the sequence of bus transactions.

54. The circuit of claim 50, wherein the sequence is a legal sequence of bus transactions and wherein the bug comprises an incorrect response to the legal sequence.